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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,363	02/17/2004	Bryan S. Shelton	EMCORE 3.0-085	1810

530 7590 09/12/2005

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EXAMINER	
WILSON, SCOTT R	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/780,363	SHELTON ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-119* is/are pending in the application.

4a) Of the above claim(s) *72-119* is/are withdrawn from consideration.

5)☒ Claim(s) *67-71* is/are allowed.

6)☒ Claim(s) *1-4,6,10,23,34,35,37,42,55 and 66* is/are rejected.

7)☒ Claim(s) *5,7-9,11-22,24-33,36,38-41,43-54 and 56-65* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/17/04, 4/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-71 in the response filed 8 July 2005 is acknowledged.

Specification

The disclosure is objected to because of the following informalities: Element labels are incorrect in the following locations:

in paragraph 0030, line 5, 104 should be 304,

in paragraph 0032, line 1, 106 should be 306,

in paragraph 0032, line 8, 106 should be 306,

in paragraph 0032, line 4, on page 13, 106 should be 306,

in paragraph 0032, line 16, on page 13, 106 should be 306,

in paragraph 0035, line 2, 108 should be 308,

and in paragraph 0038, lines 1 and 2, 110, 106, 112 and 118 should be 310, 306, 312 and 318, respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 3, 4, 6, 10 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Asano et al.. As to claim 1, Asano et al., Figure 1, discloses a semiconductor body including a lower semiconductor layer (22) and an upper semiconductor layer (23) formed atop a portion of said lower semiconductor layer, said lower semiconductor layer and said upper semiconductor layer being of a same conductivity type, said lower semiconductor layer being more highly doped than said upper semiconductor layer, said semiconductor body defining a lower contact surface, which just penetrates the lower semiconductor layer below layer (28), and a plurality of mesas projecting upwardly from said lower contact surface, said lower contact surface including at least a portion of said lower layer, each of said plurality of mesas including a portion of said upper layer and defining an upper contact surface, each of said plurality of mesas being separated from adjacent ones of said plurality of mesas by a portion of said lower contact surface; a plurality of upper metallic contacts (31a)(col. 1, lines 42-44) each disposed atop a respective one of said plurality of mesas and forming a respective Schottky contact with the upper contact surface of that mesa; and one or more lower metallic contacts (28)(col. 1, line 34) disposed on said lower contact surface in substantially ohmic contact therewith, at least part of said one or more lower metallic contacts extending between at least some of said plurality of mesas.

As to claim 3, Asano et al., Figure 1, discloses that each of the plurality of mesas includes a portion of said lower layer, embodied as the boundary between the lower and upper semiconductor layers under the mesa.

As to claim 4, Asano et al., Figure 1, discloses that each of said plurality of upper metallic contacts includes a contact metal layer (31a) that forms the respective Schottky contact with said upper contact surface and a bond pad metal layer (34) that is disposed atop said contact metal layer.

As to claim 6, Asano et al., Figure 1, discloses that the lower metallic contact region (28), especially to the right of the mesa shown in the figure, would be continuous with the neighboring mesa.

As to claim 10, Asano et al., Figure 1, discloses that the lower and upper semiconductor layers are n-type.

As to claim 23, Asano et al., Figure 1, discloses a first conductor (34) electrically connected to the upper metallic contact (31a) and a second conductor (30) electrically connected to the lower metallic contact (28).

Claims 34, 37, 42, and 55 are rejected under 35 U.S.C. 102(e) as being anticipated by Asano et al.. As to claim 34, Asano et al., Figure 1, discloses a semiconductor body including a lower semiconductor layer (22) and an upper semiconductor layer (23) formed atop a portion of said lower semiconductor layer, said lower semiconductor layer and said upper semiconductor layer being of the same conductivity type, said lower semiconductor layer being more highly doped than said upper semiconductor layer, said semiconductor body defining a lower contact surf ace, which just penetrates the lower semiconductor layer below layer (28), and a plurality of mesas projecting upwardly from said lower contact surface, said lower contact surface including a portion of said lower layer, each of said plurality of mesas including a portion of said upper layer and a further portion of said lower layer, each of said plurality of mesas defining an upper contact surface and being separated from adjacent ones of said plurality of mesas by a portion of said lower contact surface; a plurality of upper metallic contacts (31a)(col. 1, lines 42-44) each disposed atop a respective one of said plurality of mesas and forming a respective Schottky contact with the upper contact surface of that mesa; and one or more lower metallic contacts (28)(col. 1, line 34) disposed on said lower contact surface in substantially ohmic contact therewith.

As to claim 37, Asano et al., Figure 1, discloses that each of said plurality of upper metallic contacts includes a contact metal layer (31a) that forms the respective Schottky contact with said upper contact surface and a bond pad metal layer (34) that is disposed atop said contact metal layer.

As to claim 42, Asano et al., Figure 1, discloses that the lower and upper semiconductor layers are n-type.

As to claim 55, Asano et al., Figure 1, discloses a first conductor (34) electrically connected to the upper metallic contact (31a) and a second conductor (30) electrically connected to the lower metallic contact (28).

Claim 66 is rejected under 35 U.S.C. 102(e) as being anticipated by Li. Li, Figures 1A and 1B, discloses (col. 6, lines 11-24) a submount substrate; one or more first submount contacts (30), each such one or more first submount contacts being exposed at a front surface of said submount substrate; a first common terminal, embodied as two or more of the bumps (54) which may be electrically connected within the substrate (52), disposed on said front surface of said submount substrate, said first common terminal being electrically connected to said each one or more first submount contacts; at least a first conducting via (50A) extending from said front surface of said submount substrate to a back surface of said submount substrate, said first conducting via being electrically connected to said first common terminal; a first further terminal (39) disposed on said back surface of said submount substrate and configured to provide connections external to said submount structure, said first further terminal being electrically connected to said first conducting via; one or more second submount contact pads, embodied as two or more of the remaining pads (30), each such one or more second submount contact pads exposed at said front surface of said submount substrate; a second common terminal, embodied as two or more of the remaining bumps (54) disposed on said front surface of said submount substrate, said second common terminal being electrically connected to said each one or more second submount contacts; at least a second conducting via (50B) extending from said front surface of said submount substrate to said back surface of said submount substrate, said second conducting via being electrically connected to said second common terminal; and a second further terminal (44) disposed on said back surface of said submount substrate and configured to provide connections external to said submount structure, said second further terminal being electrically connected to said second conducting via.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. in view of Chiola. Asano et al., Figure 1, discloses the invention of claim 1, as described above. Asano et al. does not disclose expressly the size of each of said plurality of mesas is selected such that a forward operating voltage of said Schottky diode is minimized. Chiola, paragraph [0010], discloses a mesa region with a higher active conducting area, which is beneficial towards reducing the forward voltage drop of the device during forward conduction. At the time of invention, it would have been obvious to a person of ordinary skill in the art to increase the conducting area of each mesa. The motivation for doing so would have been to minimize the forward operating voltage of the diode. Therefore, it would have been obvious to combine Chiola with Asano et al. to obtain the invention as specified in claim 2.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. in view of Chiola. Asano et al., Figure 1, discloses the invention of claim 34, as described above. Asano et al. does not disclose expressly the size of each of said plurality of mesas is selected such that a forward operating voltage of said Schottky diode is minimized. Chiola, paragraph [0010], discloses a mesa region with a higher active conducting area, which is beneficial towards reducing the forward voltage drop of the device during forward conduction. At the time of invention, it would have been obvious to a person of ordinary skill in the art to increase the conducting area of each mesa. The motivation for doing so would have been to minimize the forward operating voltage of the diode. Therefore, it would have been obvious to combine Chiola with Asano et al. to obtain the invention as specified in claim 35.

Allowable Subject Matter

Claims 5, 7-9, 11-22, 24-33, 36, 38-41, 43-54 and 56-65 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 67-71 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

srw
September 1, 2005